1. A method for forming copper vias on a substrate, comprising:

depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the substrate;

using a photolithography technique in order to define a number of via holes above the seed layer; and

depositing a layer of copper over the seed layer using electroless plating.

2. The method of claim 1, wherein depositing a seed layer includes depositing a seed layer having a thickness of less than 15 nanometers (nm).

2 ~~3~~. The method of claim 1 ~~1~~, wherein depositing a seed layer includes depositing a seed layer using a physical vapor deposition process.

4. The method of claim 1, wherein using a photolithography technique in order to define a number of via holes above the seed layer includes patterning a photoresist layer to define the number of via holes above the seed layer.

3. ~~5~~. The method of claim 1 ~~4~~, wherein depositing a layer of copper using electroless plating includes filling the number of via holes to a top surface of the photoresist layer.

6. The method of claim 5, wherein the method further includes removing the photoresist layer using oxygen plasma ashing.

1 ~~7~~. A method for forming vias on a substrate, comprising:

depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu) having a thickness of less than 15 nanometers (nm) on the substrate;

depositing a patterned photoresist layer over the seed layer, wherein depositing the patterned photoresist layer defines a number of via holes opening to the seed layer;

depositing a layer of copper over the seed layer using electroless plating; and

removing the photoresist layer using oxygen plasma ashing.

5. ~~8.~~ A method for forming vias on a substrate, comprising:

depositing a seed layer including a thin film of Palladium (Pd) or Copper (Cu)having a discontinuous island structure on the substrate using a sputtering deposition technique;

depositing a patterned photoresist layer over the seed layer, wherein depositing the patterned photoresist layer defines a number of via holes opening to the seed layer;

depositing a layer of copper over the seed layer using electroless plating.

6. ~~9.~~ The method of claim ~~8~~ 5, wherein depositing a first seed layer having a discontinuous island structure includes a discontinuous island structure having a thickness of less than 15 nanometers (nm).

7. ~~10.~~ The method of claim ~~8~~ 5, wherein depositing a layer of copper over the seed layer includes forming a number of copper vias, wherein the number of copper vias form on the seed layer but not on the patterned photoresist layer.

8. ~~11.~~ The method of claim ~~10~~ 7, wherein forming a number of copper vias includes filling the number of via holes to a top surface of the patterned photoresist layer.

9. ~~12.~~ The method of claim ~~8~~ 5, wherein the method further includes removing the photoresist layer using oxygen plasma ashing.

Sub B1

13. A method for forming copper vias and a first metal layer, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate;

depositing a first patterned photoresist layer, wherein depositing the first patterned photoresist layer defines a number of via holes above the first seed layer;

forming a first layer of copper using electroless plating, wherein forming the first layer of copper vias using electroless plating includes filling the number of via holes to a top surface of the first patterned photoresist layer;

depositing a second seed layer including a thin film of Palladium (Pd) Copper (Cu) on the first layer of copper vias and the top surface of the photoresist layer;

depositing a second patterned photoresist layer, wherein depositing the second patterned photoresist layer defines a number of conductor line openings above the second seed layer; and

forming a second layer of copper using electroless plating, wherein depositing a second layer of copper using electroless plating includes filling the number of conductor line openings to a top surface of the second patterned photoresist layer.

11. ~~14~~. The method of claim 10 ~~13~~, wherein depositing a first seed layer includes depositing a first seed layer having a discontinuous island structure.

12. ~~15~~. The method of claim 10 ~~13~~, wherein depositing a first seed layer includes depositing a first seed layer using an evaporation deposition technique.

13 ~~16~~. The method of claim 10 ~~13~~, wherein forming a first layer of copper using electroless plating includes forming a first number of copper vias, wherein the first number of copper vias form on the first seed layer but not on the first patterned photoresist layer.

14. ~~17.~~ The method of claim 10 ~~13,~~ wherein depositing the second seed layer includes depositing the second seed layer using a physical vapor deposition process.

15 ~~18.~~ The method of claim 10 ~~13,~~ wherein depositing a second patterned photoresist layer includes depositing a second patterned photoresist layer which has a thickness which is less that a thickness of the first patterned photoresist layer.

sub b2

19. The method of claim 13, wherein depositing the second patterned photoresist layer which defines a number of conductor line openings includes a number of first level metal line openings.

20. A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer on a substrate;

patterning a first photoresist layer over the first seed layer to define a number of via holes opening to the first seed layer;

forming a first level of copper vias in the number of via holes using electroless plating;

depositing a second seed layer on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a number of conductor line openings to the second seed layer;

forming a first level of conductor lines in the number of conductor line openings using electroless plating;

depositing a third seed layer on the first level of conductor lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a number of via holes opening to the third seed layer; and

forming a second level of copper vias in the number of via holes using electroless plating.

21. The method of claim 20, wherein the method further comprises:

depositing a fourth seed layer on the second level of copper vias and third photoresist layer;

patterning a fourth photoresist layer over the fourth seed layer to define a number of conductor line openings to the fourth seed layer; and

forming a second level of conductor lines in the number of conductor line openings using electroless plating.

22. The method of claim 21, wherein depositing the first seed layer includes depositing a first seed layer having a discontinuous island structure.

23. The method of claim 22, wherein depositing a first seed layer having a discontinuous island structure includes depositing a discontinuous island structure of Palladium (Pd) or Copper (Cu).

sub B3

24. The method of claim 21, wherein forming a first level of copper vias in the number of via holes using electroless plating includes forming the number of copper vias on the seed layer but not on the first photoresist layer.

25. The method of claim 21, wherein depositing a first seed layer includes depositing a first seed layer having a thickness of less than 15 nanometers (nm).

26. The method of claim 21, wherein depositing the first seed layer includes depositing the first seed layer using a physical vapor deposition process.

27. The method of claim 21, wherein patterning a second photoresist layer over the second seed layer includes patterning a second photoresist layer having a thickness which is less than a thickness of the first photoresist layer.

28. A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate using a physical vapor deposition process;

patterning a first photoresist layer over the first seed layer to define a number of via holes opening to the first seed layer;

forming a first level of copper vias in the number of via holes using electroless plating;

depositing a second seed layer on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a number of conductor line openings to the second seed layer;

forming a first level of copper lines in the number of conductor line openings using electroless plating;

depositing a third seed layer on the first level of copper lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a number of via holes opening to the third seed layer;

forming a second level of copper vias in the number of via holes using electroless plating; and

removing the first, second, and third photoresist layers using oxygen plasma etching.

29. The method of claim 28, wherein depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate using a physical vapor deposition process includes using an evaporation deposition technique.

30. The method of claim 28, wherein removing the first, second, and third photoresist layers using oxygen plasma etching includes removing the first, second, and third seed layers.

31. The method of claim 28, wherein depositing a second and a third seed layer includes depositing a second and third seed layer having a discontinuous island structure.

32. The method of claim 31, wherein depositing a second and a third seed layer having a discontinuous island structure includes depositing a second and a third seed layer using a sputtering deposition technique.

33. The method of claim 32, wherein depositing a second and a third seed layer includes depositing a second and a third seed layer having a thickness of less than 15 nanometers (nm).

34. A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate;

patterning a first photoresist layer over the first seed layer to define a number of via holes opening to the first seed layer;

forming a first level of copper vias in the number of via holes using electroless plating;

depositing a second seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a number of conductor line openings to the second seed layer;

forming a first level of copper lines in the number of conductor line openings using electroless plating;

depositing a third seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first level of copper lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a number of via holes opening to the third seed layer; and

forming a second level of copper vias in the number of via holes using electroless plating;

depositing a fourth seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the second level of copper vias and third photoresist layer;

patterning a fourth photoresist layer over the fourth seed layer to define a number of conductor line openings to the fourth seed layer; and

forming a second level of copper lines in the number of conductor line openings using electroless plating.

35. The method of claim 34, wherein the depositing the first, second, third, and fourth seed layers includes depositing a first, second, third, and fourth seed layer having a discontinuous island structure.

36. The method of claim 35, wherein depositing a first, second, third, and fourth seed layer having a discontinuous island structure includes depositing a first, second, third, and fourth seed layer using a sputtering deposition technique.

37. The method of claim 36, wherein depositing a first, second, third, and fourth seed layer having a discontinuous island structure includes depositing a first, second, third, and fourth seed layer having thickness of less than 10 nanometers (nm).

38. The method of claim 34, wherein the method further includes removing the first, second, third, and fourth photoresist layers using an oxygen plasma etching.

39. The method of claim 38, wherein removing the first, second, third, and fourth photoresist layers using an oxygen plasma etching includes removing the first, second, third, and fourth seed layers.

40. The method of claim 39, wherein the further includes forming a thin diffusion barrier on the first and the second number of copper vias and the first level and the second level of copper lines.

41. The method of claim 40, wherein forming a thin diffusion barrier includes forming a thin diffusion barrier of Tungsten Silicon Nitride (WSi_xN_y) having a thickness of less than 8 nanometers (nm).

42. The method of claim 41, wherein forming a thin diffusion barrier of Tungsten Silicon Nitride (WSi_xN_y) having a thickness of less than 8 nanometers (nm) includes forming a graded composition of WSi_x, where x varies from 2.0 to 2.5, and nitriding the graded composition of WSi_x.

43. An integrated circuit, comprising:

at least one semiconductor device formed in a substrate;

a first number of seed layers including a thin film of Palladium (Pd) or Copper formed on a number of portions of the at least one semiconductor device;

a number of copper vias formed above and contacting the first number of seed layers;

a second number of seed layers including a thin film of Palladium (Pd) or Copper formed on the number of copper vias; and

a number of conductor metal lines formed above and contacting second number of seed layers.

44. The integrated circuit of claim 43, wherein the integrated circuit further includes a thin diffusion barrier covering the number of copper vias, the number of conductor metal lines, and the first and the second number of seed layers.

45. The integrated circuit of claim 44, wherein the thin diffusion barrier has a thickness of less than 8.0 nanometers (nm).

46. The integrated circuit of claim 43, wherein the first number of seed layers have a thickness of less than 15 nanometers (nm).

47. The integrated circuit of claim 43, wherein the first number of seed layers includes a first number of seed layers having a discontinuous island structure.

48. The integrated circuit of claim 43, wherein the number of conductor metal lines includes a number of copper metal lines.

49. An integrated circuit, comprising:

a substrate including at least one transistor;

a first number of seed layers including a thin film of Palladium (Pd) or Copper having a thickness of less than 15 nanometers (nm), formed on a source and a drain region of the at least one transistor;

a number of copper vias formed above and contacting the first number of seed layers;

a second number of seed layers including a thin film of Palladium (Pd) or Copper formed on the number of copper vias; and

a number of copper metal lines formed above and contacting the number of second number of seed layers.

50. The integrated circuit of claim 49, wherein the integrated circuit further includes a thin diffusion barrier, having a thickness of less than 8.0 nanometers (nm), covering the number of copper vias, the number of copper metal lines, and the first and the second number of seed layers.

51. The integrated circuit of claim 50, wherein the thin diffusion barrier includes a graded composition of Tungsten Silicon Nitride (WSi_xN_y), and wherein x varies from 2.0 to 2.5.

52. The integrated circuit of claim 49, wherein the second number of seed layers includes a second number of seed layers having a discontinuous island structure with an island thickness in the range of 3 to 10 nanometers.

53. An integrated circuit, comprising:

at least one semiconductor device formed in a substrate;

a first number of seed layers including a thin film of Palladium (Pd) or Copper, having a discontinuous island structure which has a thickness in the range of 3 to 10 nanometers, formed on a number of portions of the at least one semiconductor device;

a number of copper vias formed above and contacting the first number of seed layers;

a second number of seed layers including a thin film of Palladium (Pd) or Copper formed on the number of copper vias;

a number of copper metal lines formed above and contacting the number of second number of seed layers; and

a thin diffusion barrier, having a thickness of less than 8.0 nanometers, covering the number of copper vias, the number of copper metal lines, and the first and the second number of seed layers.

54. The integrated circuit of claim 53, wherein the thin diffusion barrier includes a graded composition of Tungsten Silicon Nitride (WSi_xN_y), and wherein x varies from 2.0 to 2.5.

55. The integrated circuit of claim 53, wherein the second number of seed layers includes a second number of seed layers having a discontinuous island structure with an island thickness in the range of 3 to 10 nanometers.

56. The integrated circuit of claim 53, wherein the thin diffusion barrier has a thickness in the range of 2.0 to 6.0 nanometers.

57. A multilayer copper wiring structure, comprising:

at least one semiconductor device formed in a substrate;

a first number of seed layers including a thin film of Palladium (Pd) or Copper formed on a number of portions of the at least one semiconductor device;

a first level of copper vias formed above and contacting the first number of seed layers;

a second number of seed layers including a thin film of Palladium (Pd) or Copper formed on the first level of copper vias;

a first level of copper metal lines formed above and contacting second number of seed layers;

a third number of seed layers including a thin film of Palladium (Pd) or Copper formed on the first level of copper metal lines;

a second level of copper vias formed above and contacting the third number of seed layers;

a fourth number of seed layers including a thin film of Palladium (Pd) or Copper formed on the second level of copper vias; and

a second level of copper metal lines formed above and contacting fourth number of seed layers.

58. The multilayer copper wiring structure of claim 57, wherein the structure further includes a thin diffusion barrier, having a thickness of less than 8.0 nanometers (nm), covering the first and the second level of copper vias, the first and

the second level of copper metal lines, and the first, second, third, and fourth number of seed layers.

59. The multilayer copper wiring structure of claim 57, wherein the thin diffusion barrier includes a graded composition of Tungsten Silicon Nitride (WSi_xN_y), and wherein x varies from 2.0 to 2.5.

60. The multilayer copper wiring structure of claim 57, wherein the first, second, third, and fourth number of seed layers include a discontinuous island structure with an island thickness in the range of 3 to 10 nanometers.

61. A multilayer copper wiring structure, comprising:

a substrate including at least one transistor;

a first number of seed layers including a thin film of Palladium (Pd) or Copper, having a thickness of less than 15 nanometers (nm), formed on a source and a drain region of the at least one transistor;

a first level of copper vias formed above and contacting the first number of seed layers;

a second number of seed layers including a thin film of Palladium (Pd) or Copper, having a thickness of less than 15 nanometers (nm), formed on the first level of copper vias;

a first level of copper metal lines formed above and contacting second number of seed layers;

a third number of seed layers including a thin film of Palladium (Pd) or Copper, having a thickness of less than 15 nanometers (nm), formed on the first level of copper metal lines;

a second level of copper vias formed above and contacting the third number of seed layers;

a fourth number of seed layers including a thin film of Palladium (Pd) or Copper, having a thickness of less than 15 nanometers (nm), formed on the second level of copper vias;

a second level of copper metal lines formed above and contacting fourth number of seed layers; and

a thin diffusion barrier, having a thickness of less than 8.0 nanometers, covering the first and the second level of copper vias, the first and the second level of copper metal lines, and the first, second, third, and fourth number of seed layers.

62. The multilayer copper wiring structure of claim 61, wherein the thin diffusion barrier includes a graded composition of Tungsten Silicon Nitride (WSi_xN_y), and wherein x varies from 2.0 to 2.5.

63. The multilayer copper wiring structure of claim 61, wherein the first, second, third, and fourth number of seed layers include a discontinuous island structure with an island thickness in the range of 3 to 10 nanometers.

64. The multilayer copper wiring structure of claim 61, wherein the thin diffusion barrier has a thickness in the range of 2.0 to 6.0 nanometers.